9-BIT SHIFT REGISTER

## FEATURES

■ 700MHz min. shift frequency
■ Extended 100E Vee range of -4.2 V to -5.5 V
■ 9 bits wide for byte-parity applications
■ Asynchronous Master Reset
■ Dual clocks
■ Fully compatible with industry standard 10KH, 100K ECL levels

- Internal $75 \mathrm{~K} \Omega$ input pulldown resistors

■ Fully compatible with Motorola MC10E/100E142
■ Available in 28 -pin PLCC package

## BLOCK DIAGRAM



## DESCRIPTION

The SY10/100E142 are high-speed 9-bit shift registers designed for use in new, high-performance ECL systems. The E142 can accept serial or parallel data to be shifted out in one direction as both serial and parallel outputs. The nine inputs, Do-D8, accept parallel input data, while S-IN accepts serial input data.
The SEL (Select) control pin serves to determine the mode of operation, either SHIFT or LOAD. The shift direction is from bit 0 to bit 8 . The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK1 or CLK2. Shifting is also performed on the rising edge of either CLK1 or CLK2. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E142 is designed for applications such as diagnostic scan registers, parallel-to-serial conversions and is also suitable for byte-wide parity.

## PIN NAMES

| Pin | Function |
| :--- | :--- |
| Do-D8 | Parallel Data Inputs |
| S-IN | Serial Data Input |
| SEL | Mode Select Input |
| CLK1, CLK2 | Clock Inputs |
| MR | Master Reset |
| Q0-Q8 | Data Outputs |
| Vcco | Vcc to Output |

## PACKAGE/ORDERING INFORMATION

## Ordering Information ${ }^{(1)}$



28-Pin PLCC (J28-1)

| Part Number | Package <br> Type | Operating <br> Range | Package <br> Marking | Lead <br> Finish |
| :--- | :---: | :---: | :---: | :---: |
| SY10E142JC | J28-1 | Commercial | SY10E142JC | Sn-Pb |
| SY10E142JCTR ${ }^{(2)}$ | J28-1 | Commercial | SY10E142JC | Sn-Pb |
| SY100E142JC | J28-1 | Commercial | SY100E142JC | Sn-Pb |
| SY100E142JCTR | $(2)$ | J28-1 | Commercial | SY100E142JC |
| SY10E142JY(3) | $\mathrm{J} 28-1$ | Industrial | SY-Pb <br> Pb-Free bar-line indicator | Matte-Sn |
| SY10E142JYTR ${ }^{(2,3)}$ | J28-1 | Industrial | SY10E142JY with <br> Pb-Free bar-line indicator | Matte-Sn |
| SY100E142JZ ${ }^{(3)}$ | J28-1 | Commercial | SY100E142JZ with <br> Pb-Free bar-line indicator | Matte-Sn |
| SY100E142JZTR ${ }^{(2,3)}$ | J28-1 | Commercial | SY100E142JZ with <br> Pb-Free bar-line indicator | Matte-Sn |

## Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_{A}=25^{\circ} \mathrm{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb -Free package is recommended for new designs.

## TRUTH TABLE

| SEL | MODE |
| :---: | :---: |
| $L$ | LOAD |
| $H$ | SHIFT |

## DC ELECTRICAL CHARACTERISTICS

Vee = Vee (Min.) to Vee (Max.); $\mathrm{Vcc}=\mathrm{Vcco}=\mathrm{GND}$

| Symbol | Parameter | $\mathrm{TA}=0^{\circ} \mathrm{C}$ |  |  | TA $=+25^{\circ} \mathrm{C}$ |  |  | TA $=+85^{\circ} \mathrm{C}$ |  |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. |  |  |
| IIH | Input HIGH Current | - | - | 150 | - | - | 150 | - | - | 150 | $\mu \mathrm{A}$ | - |
| Iee | Power Supply Current ${ }_{10 \mathrm{E}}^{10 \mathrm{E}}$ | - | $\begin{aligned} & 120 \\ & 120 \end{aligned}$ | $\begin{aligned} & 145 \\ & 145 \end{aligned}$ | - | $\begin{aligned} & 120 \\ & 120 \\ & \hline \end{aligned}$ | $\begin{aligned} & 145 \\ & 145 \\ & \hline \end{aligned}$ | - | $\begin{aligned} & 120 \\ & 138 \end{aligned}$ | $\begin{array}{r} 145 \\ 165 \\ \hline \end{array}$ | mA | - |

## AC ELECTRICAL CHARACTERISTICS

Vee = Vee (Min.) to Vee (Max.); $\mathrm{Vcc}=\mathrm{Vcco}=\mathrm{GND}$

| Symbol | Parameter | $\mathrm{TA}=0^{\circ} \mathrm{C}$ |  |  | $\mathrm{TA}=+25^{\circ} \mathrm{C}$ |  |  | $\mathrm{TA}=+85^{\circ} \mathrm{C}$ |  |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. |  |  |
| fSHIFT | Max. Shift Frequency | 700 | 900 | - | 700 | 900 | - | 700 | 900 | - | MHz | - |
| tPD | Propagation Delay to Output CLK <br> MR | $\begin{aligned} & 600 \\ & 600 \end{aligned}$ | $\begin{aligned} & 800 \\ & 800 \end{aligned}$ | $\begin{aligned} & 1000 \\ & 1000 \end{aligned}$ | $\begin{aligned} & 600 \\ & 600 \end{aligned}$ | $\begin{aligned} & 800 \\ & 800 \end{aligned}$ | $\begin{aligned} & 1000 \\ & 1000 \end{aligned}$ | $\begin{aligned} & 600 \\ & 600 \end{aligned}$ | $\begin{aligned} & 800 \\ & 800 \end{aligned}$ | $\begin{aligned} & 1000 \\ & 1000 \end{aligned}$ | ps | - |
| ts | Set-up Time <br> D <br> SEL | $\begin{gathered} 50 \\ 300 \end{gathered}$ | $\begin{gathered} -100 \\ 150 \end{gathered}$ | - | $\begin{array}{\|c\|} 50 \\ 300 \end{array}$ | $\begin{gathered} -100 \\ 150 \end{gathered}$ | - | $\begin{gathered} 50 \\ 300 \end{gathered}$ | $\begin{gathered} -100 \\ 150 \end{gathered}$ | - | ps | - |
| tH | Hold Time <br> D <br> SEL | $\begin{gathered} 300 \\ 75 \end{gathered}$ | $\begin{gathered} 100 \\ -150 \end{gathered}$ | - | $\begin{array}{\|c} 300 \\ 75 \end{array}$ | $\begin{gathered} 100 \\ -150 \end{gathered}$ | - | $\begin{gathered} 300 \\ 75 \end{gathered}$ | $\begin{gathered} 100 \\ -150 \end{gathered}$ | - | ps | - |
| tRR | Reset Recovery Time | 900 | 700 | - | 900 | 700 | - | 900 | 700 | - | ps | - |
| tPW | Minimum Pulse Width CLK, MR | 400 | - | - | 400 | - | - | 400 | - | - | ps | - |
| tskew | Within-Device Skew | - | 75 | - | - | 75 | - | - | 75 | - | ps | 1 |
| $\begin{aligned} & \mathrm{tr} \\ & \mathrm{tf} \end{aligned}$ | Rise/Fall Time $20 \%$ to $80 \%$ | 300 | 525 | 800 | 300 | 525 | 800 | 300 | 525 | 800 | ps | - |

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.

## 28-PIN PLCC (J28-1)



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